AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A master/slave synchronization communication system, comprising:

a single master and a single or a plurality of slaves that are based on IEEE1394,

wherein the master/slave synchronization communication system has a communication period which is set to an integral multiple of a natural period of IEEE1394 communications with the natural period considered as a base cycle,

each of the master and the slaves has a detecting section ~~of~~ for detecting a synchronization point being a start timing of the communication period, and a base cycle counter which shows what base cycle number [[the]] a present cycle is from the synchronization point,

the master has a transmission management table in which destination slaves ~~of~~ for receiving instruction data are previously allocated to each of the base cycle counter values, and transmits instruction data to each slave every time the base cycle counter is updated based on the transmission management table, and

each of the slaves has transmission timing information in which a response cycle value for transmitting response data is previously stored, and transmits response data to the master when ~~the pre-allocated~~ a value of the base cycle counter ~~is reached~~ reaches the response cycle value stored in the transmission timing information.

2. (currently amended): The master/slave synchronization communication system according to claim 1,

wherein as the detecting section of the synchronization point,

the master determines an arbitrary base cycle as a synchronization point, and transmits instruction data to each slave based on the base cycle, [[and]]

the transmission timing information of each of the slaves includes an instruction cycle value in which the instruction data is to be received from the master, and

each of the slaves corrects, when the instruction data is received, a current value of the base cycle counter based on ~~the base cycle counter value assumed when the instruction data is received and the pre-allocated base cycle counter value assumed when the instruction data is received~~ the instruction cycle value included in the transmission timing information, and detects a time as a synchronization point when the count value reaches a predetermined value.

3. (currently amended): The master/slave synchronization communication system according to claim 1,

wherein as the detecting section of the synchronization point,

the master determines an arbitrary base cycle as a synchronization point, and writes CYCLE_TIME register value as the next synchronization point in the instruction data when the master transmits instruction data to each slave based on the base cycle, and

each of the slaves corrects, when the instruction data is received, a current value of the base cycle counter value based on the CYCLE_TIME register value ~~as the next synchronization point~~ written in the instruction data ~~assumed when the instruction data is received~~ and the current register value of its own CYCLE_TIME register value, and detects a time as a synchronization point when the count value reaches a predetermined value.

4. (original): The master/slave synchronization communication system according to claim 1,

wherein as the detecting section of the synchronization point,

the master determines an arbitrary base cycle as a synchronization point, sets the base cycle counter value to a predetermined value, and transmits the present base cycle counter value to each slave when the master transmits an instruction to the each slave, and

each of the slaves sets the base cycle counter value to its own base cycle counter, and detects a time as a synchronization point when the count value reaches a predetermined value.

5. (original): The master/slave synchronization communication system according to claim 1,

wherein as the detecting section of the synchronization point,

the master detects a synchronization point based on CYCLE_TIME register value, and simultaneously sets the base cycle counter value to a predetermined value, and

each of the slave detects a synchronization point based on the CYCLE_TIME register value by way of the same way as the master, and simultaneously sets the base cycle counter value to a predetermined value.